Amendments to Specification

Please amend the paragraph starting at page 3, line 20, as follows:

The present invention is close to the second class of filter discussed above using an ARMA design. A variable equivalent sample rate recursive coefficient converter (VESRCC), shown in Fig. 1 and described in more detail in ~~co-pending~~ U.S. Patent ~~Application Serial No. 09/925,546 filed August 8, 2001~~ No. 6,976,045, issued on December 30, 2005 to Kevin Ferguson and entitled "Variable Sample Rate Recursive Digital Filter", is used which takes advantage of the bilinear transform to shift the poles of the IIR filters. Referring now to Fig. 2 a variable passband ARMA filter **10** is shown that meets the IEEE P205 luminance filter specification (IEEE G 2.1.4/98-07: "IEEE P205 Draft Standard on Television Measurement of Luminance Signal Levels"). The architecture shown uses a sum of weighted first order IIR filters, similar to the "seagull" architecture disclosed in co-pending U.S. Patent Application Serial No. ~~[DF 7773]~~ 10/802,305 filed March 17, 2004 by Kevin Ferguson and entitled "UpSampling Half-Band Reconstruction Filtering". X(n) represents an input signal (forward signal), and X(N-n) represents a reversed version of the input signal (reverse signal). The forward signal is input to a first IIR filter **20**, the reverse signal is input to a second IIR filter **30** in parallel with the first IIR filter, and the outputs from the two filters are combined with the input signal in a summing circuit **40**. The variable coefficients for the ARMA filter **10** are derived from initial filter values, $\mathbf{b_0}$ and $\mathbf{a_1}$, via respective VESRCC circuits **50, 60**, to which also are input an equivalent passband ratio, **R**. By varying the parameter **R** a continuous range from full bandwidth to some small fraction of nominal bandwidth is achieved.

Please amend the paragraph starting at page 5, line 1 as follows:

In an ARMA filter, such as that of Fig. 2, if the zeroes are shifted, misalignment of zero and pole related gains over frequency cause response distortions in the general case. For example, higher frequency stop band attenuation may suffer as the zero shifts lower in the frequency domain. However if for zeroes the bilinear transform based on the scaling method implemented by the VESRCC circuits **50, 60** is applied above a nominal frequency resampling rate, corresponding to a resampling rate R>1.0 in the above-mentioned ~~co-pending application 09/925,546~~ U.S. Patent No. 6,976,045, the response distortion is mitigated. Below the nominal resampling rate (R<1.0), the zeroes no longer shift, but instead are nominal. This allows the advantages of the VESRCC circuits **50, 60**, as cited in the ~~co-pending application~~ above-mentioned U.S. Patent No. 6,976,045, while solving the problem of zero/pole gain mismatches, such as stop band attenuation reduction mentioned above. The present invention uses the asymmetric (R>1.0 only) use of the VESRCC circuit **50** on zeroes only, and the symmetric (all values of R) use of the VESRCC circuit **60** on poles.